LX –TI DM8148 Technical Documentation

User Guide

09/10/2012

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LX TI DM8148 User Guide

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1. HARDWARE

1.1 Front View

Item	Definition
1. Power button	Switch to power on or power off the system.
2. USB ports	Connect to USB device.
3. Mic-in connector	Connect to microphone.
4. Line-out connector	Connect to speaker.

1.2 Rear View

Item	Definition
5. USB ports	Connect to USB device.
6. RJ45 connector	Connect to 10/100/1000 Base-T Ethernet
7. DVI-I connector	Connect to DVI monitor
8. DVI-D connector	Connect to DVI monitor
9. DC power jack	12V DC in.
10. Kensington lock	Case security.

Notice: Always place the system in vertical position.

"Excessive sound pressure from earphones and headphones can cause hearing loss. Adjustment of the equalizer to maximum increases the earphones and headphones output voltage and therefore the sound pressure level"

Copyright

FCC Note

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiated radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

--Reorient or relocate the receiving antenna.

--Increase the separation between the equipment and receiver.

--Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

--Consult the dealer or an experienced radio/TV technician for help. Shielded interface cables must be used in order to comply with emission limits.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Tested to Comply with FCC Standards

FOR HOME OR OFFICE USE

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2. Motherboard

TI DM8148 1GHz ARM Processor based RemoteFX / HDX / PCoIP Thin Client motherboard.
Feature :

(1) TI DM8148 with 1GHz ARM CPU support RemoteFX/ HDX/ PCoIP
(2) Dual RemoteFX Displays via HDMI to DVI-I and DVI-D
(3) Four USB ports (with USB hub chip)
(4) Optional WLAN module (reserved)
(5) Ultra-light and fanless design for a longer useful lifespan and energy efficiency
(6) Embedded platform for IT security
(7) ErP 2013 specification off mode 0.5W
(8) Applications: HD Video Conferencing, Video Surveillance DVRs, Digital Signage, Media Players/ Adapters, Mobile Medical Imaging, Network Projectors, etc.

2.1 Specification

Model no.		**LX TI DM8148 Motherboard**
Processor		TI DM8148 with 1GHz ARM CPU (support RemoteFX/ HDX/ PCoIP)
Memory		Onboard DDR3 32-bit 800/1066 MHz 512MB/1GB
Display		High performance GPU integrated, with 3D graphics engine Resolution up to 1920 x 1200 @ 60GHz
Audio Codec		TI TLV320AIC3104 (support HD audio, Line-out and Mic-in)
Storage		Onboard eMMC NAND Flash (2GB/4GB)
Networking	LAN	Realtek RTL8111E, support WOL
	WLAN	1 x Internal USB connector (optional)
Edge I/O Ports		4 x USB 2.0 ports
		1 x DVI-I connector
		1 x DVI-D connector

			1 x Audio Mic-in jack
			1 x Audio line-out jack (speaker out jack)
			1 x LAN connector (RJ-45, 10/100/1000 Base T)
			1 x 12 V DC-in jack
Internal Connectors			1 x 1*2 pins header for internal speaker
			1 x 1*2 pins header for battery
			1 x 1*2 pins header for buzzer
			1 x 1*6 pins internal USB connector for WLAN module (optional)
Power	Power Supply		24W, DC 12V /2A external power adapter
Software support	OS		Linux / Ubuntu
	Bootloader		x-loader/ u-boot
Physical Characteristics	Dimension / Weight	Motherboard	130(L) x 120(W) x 17.8(H) mm / NW : TBD
		Package	TBD
Environment	Temperature	Operation	32° to 95° F (0° to 35° C)
		Storage	-4° to 140° F (-20° to 60° C)
Regulatory Compliance			CE / FCC

Specifications subject to change without notice.

2.2 Main Chipset

Features

- High-Performance DaVinci™ Digital Media Processors

– Up to 1-GHz ARM® Cortex™-A8 RISC MPU – Up to 750-MHz C674x™ VLIW DSP

– Up to 6000/4500 C674x™ MIPS/MFLOPS

– Fully Software-Compatible with C67x+™, C64x+™

- ARM® Cortex™-A8 Core

– ARMv7 Architecture

- In-Order, Dual-Issue, Superscalar Microprocessor Core
- NEON™ Multimedia Architecture
- Supports Integer and Floating Point
- Jazelle® RCT Execution Environment
- ARM® Cortex™-A8 Memory Architecture – 32K-Byte Instruction and Data Caches

– 512K-Byte L2 Cache

– 64K-Byte RAM, 48K-Byte Boot ROM

- TMS320C674x™ Floating-Point VLIW DSP – 64 General-Purpose Registers (32-Bit)

– Six ALU (32-/40-Bit) Functional Units

- Supports 32-Bit Integer, SP (IEEE Single Precision/32-Bit)and DP(IEEE Double Precision/64-Bit) Floating Point
- Supports up to Four SP Adds Per Clock and Four DP Adds Every Two Clocks
- Supports up to Two Floating-Point(SP or DP)Approximate Reciprocal or Square Root Operations Per Cycle

– Two Multiply Functional Units

- Mixed-Precision IEEE Floating-Point

Multiply Supported up to:

– 2 SP x SP → SP Per Clock

– 2 SP x SP → DP Every Two Clocks – 2 SP x DP → DP Every Three Clocks – 2 DP x DP → DP Every Four Clocks

- Fixed-Point Multiply Supports Two 32 x 32 Multiplies, Four 16 x 16-bit Multiplies including Complex Multiplies, or Eight 8 x 8-Bit Multiplies per Clock Cycle
- C674x™ Two-Level Memory Architecture

– 32K-Byte L1P RAM/Cache With EDC – 32K-Byte L1D RAM/Cache

– 256K-Byte L2 Unified Mapped RAM/Caches With ECC

• DSP/EDMA Memory Management Unit (DEMMU)
– Maps C674x DSP and EDMA TC Memory Accesses to System Addresses
• 128K-Bytes On-Chip Memory Controller (OCMC) RAM
• Imaging Subsystem (ISS) – Camera Sensor Connection
• Parallel Connection for Raw (up to 16-Bit) and BT.656/BT.1120 (8-/16-bit) – Image Sensor Interface (ISIF) for Handling Image/Video Data From the Camera Sensor
– Resizer
• Resizing Image/Video From 1/16x to 8x
• Generating Two Different Resizing Outputs Concurrently
• Programmable High-Definition Video Image Coprocessing (HDVICP v2) Engine
– H.264, MPEG2, VC1, MPEG4, SP/ASP, JPEG/MJPEG
• Media Controller
– Controls the HDVPSS, HDVICP2, and ISS
• SGX530 3D Graphics Engine – Delivers up to 18 MPoly/sec
– Universal Scalable Shader Engine
– Direct3D Mobile, OpenGLES 1.1 and 2.0, OpenVG 1.0, OpenMax API Support
– Advanced Geometry DMA Driven Operation – Programmable HQ Image Anti-Aliasing
• Endianness
– ARM/DSP Instructions/Data – Little Endian
• HD Video Processing Subsystem (HDVPSS) – Two 165 MHz HD Video Capture Inputs
• 8-bit SD Capture Ports
• One 8/16/24-bit Input
• One 8-bit Input
– Two 165 MHz HD Video Display Outputs
• One 16/24/30-bit and one 16/24-bit Output
– Composite or S-Video Analog Output – MacroVisionSupport Available
– Digital HDMI 1.3 transmitter With Integrated PHY

– Advanced Video Processing Features Such as Scan/Format/Rate Conversion – Three Graphics Layers and Compositors

• Dual 32-bit LPDDR/DDR2/DDR3 SDRAM Interfaces – Supports up to LPDDR-400, DDR2-800, and DDR3-800 – Up to Eight x 8 Devices Total 2 GB Total Address Space – Dynamic Memory Manager (DMM)

• Programmable Multi-Zone Memory Mapping and Interleaving

• Enables Efficient 2D Block Accesses

• Supports Tiled Objects in 0°, 90°, 180°, or 270° Orientation and Mirroring

• Optimizes Interlaced Accesses

• General Purpose Memory Controller (GPMC)

– 8-/16-bit Multiplexed Address/Data Bus

– 512M-Byte Total Address Space Divided Among up to 8 Chip Selects

– Glueless Interface to NOR Flash, NAND Flash (BCH/Hamming Error Code Detection), SRAM and Pseudo-SRAM

– Error Locator Module (ELM) Outside of GPMC to Provide Upto 16-Bit/512-Bytes Hardware ECC for NAND

– Flexible Asynchronous Protocol Control for Interface to FPGA , CPLD , ASICs(EDMA) Controller

• Enhanced Direct-Memory-Access (EDMA) Controller – Four Transfer Controllers

– 64/8 Independent DMA/QDMA Channels

• Dual Port Ethernet (10/100/1000 Mb/s) With Optional Switch – IEEE 802.3 Compliant (3.3V I/O Only)

– MII/RMII/GMII/RGMII Media Independent I/Fs – Management Data I/O (MDIO) Module

– Reset Isolation

– IEEE-1588 Time-Stamping and Industrial Ethernet Protocols

• Dual USB 2.0 Ports With Integrated PHYs

– USB2.0 High-/Full-Speed Clients

– USB2.0 High-/Full-/Low-Speed Hosts, or OTG – Supports End Points 0-15

• One PCI Express 2.0 Port With Integrated PHY – Single Port With 1 Lane at 5.0 GT/s

– Configurable as Root Complex or Endpoint

• Eight 32-bit General-Purpose Timers (Timer1–8)

• One System Watchdog Timer (WDT 0)

• Six Configurable UART/IrDA/CIR Modules – UART0 With

Modem Control Signals

– Supports up to 3.6864 Mbps UART0/1/2 – Supports up to 12 Mbps UART3/4/5

– SIR, MIR, FIR (4.0 MBAUD), and CIR

• Four Serial Peripheral Interfaces (SPIs) [up to 48-MHz] – Each With Four Chip-Selects

• Three MMC/SD/SDIO Serial Interfaces [up to 48-MHz] – Three Supporting up to 1-/4-/8-Bit Modes

• Dual Controller Area Network (DCAN) Modules

– CAN Version 2 Part A, B

• Four Inter-Integrated Circuit (I2C Bus™) Ports

• Six Multi-Channel Audio Serial Ports(McASP) – Dual Ten Serializer Transmit/Receive Ports

– Quad Four Serializer Transmit/Receive Ports – DIT-Capable For S/PDIF (All Ports)

• Multi-Channel Buffered Serial Port (McBSP) – Transmit/Receive Clocks up to 48 MHz

– Two Clock Zones and Two Serial Data Pins – Supports TDM, I2S, and Similar Formats

• Serial ATA (SATA) 3.0 Gbps Controller With Integrated PHY – Direct Interface to One Hard Disk Drive

– Hardware-Assisted Native Command Queuing (NCQ) from up to 32 Entries – Supports Port Multiplier and Command-Based Switching

• Real-Time Clock (RTC)

– One-Time or Periodic Interrupt Generation

• Up to 128 General-Purpose I/O (GPIO) Pins

• One Spin Lock Module with up to 128 Hardware Semaphores

• One Mailbox Module with 12 Mailboxes

• On-Chip ARM ROM Bootloader (RBL)

• Power, Reset, and Clock Management

– SmartReflex™ Technology (Level 2b)

– Multiple Independent Core Power Domains – Multiple Independent Core Voltage Domains

– Support for Three Operating Points (OPP120/100/50) per Voltage Domain – Clock Enable/Disable Control for Subsystems and Peripherals

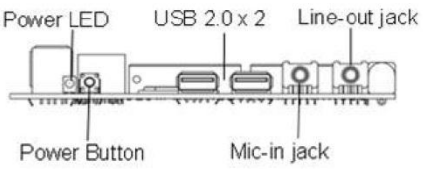
• 32KB Embedded Trace Buffer™ (ETB™) and 5-pin Trace Interface for Debug

• IEEE-1149.1 (JTAG) Compatible

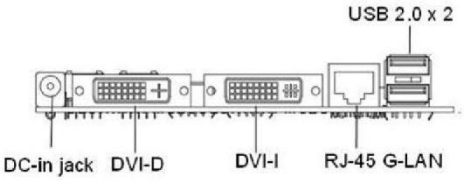
- 684-Pin Pb-Free BGA Package (CYE Suffix), 0.8-mm Ball Pitch With Via Channel™ Technology to Reduce PCB Cost
- 45-nm CMOS Technology

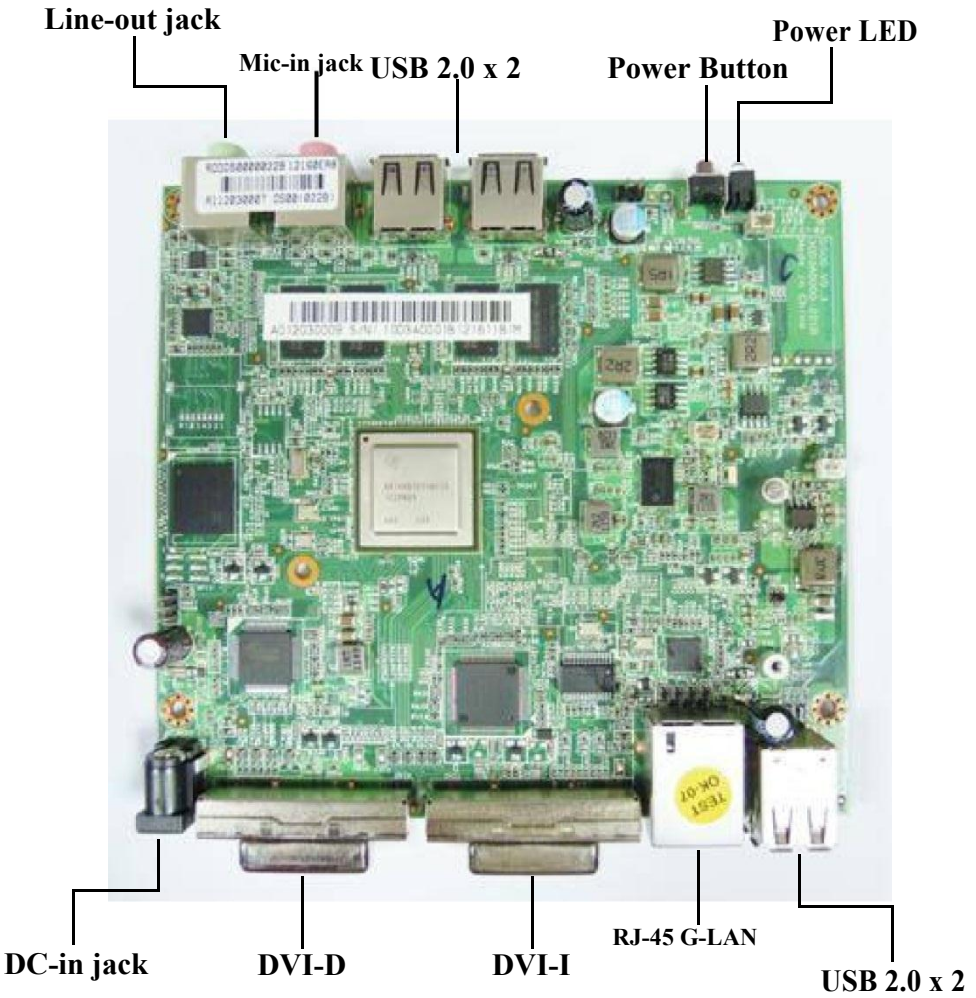
2.3 Edge I/O View

Front Side View

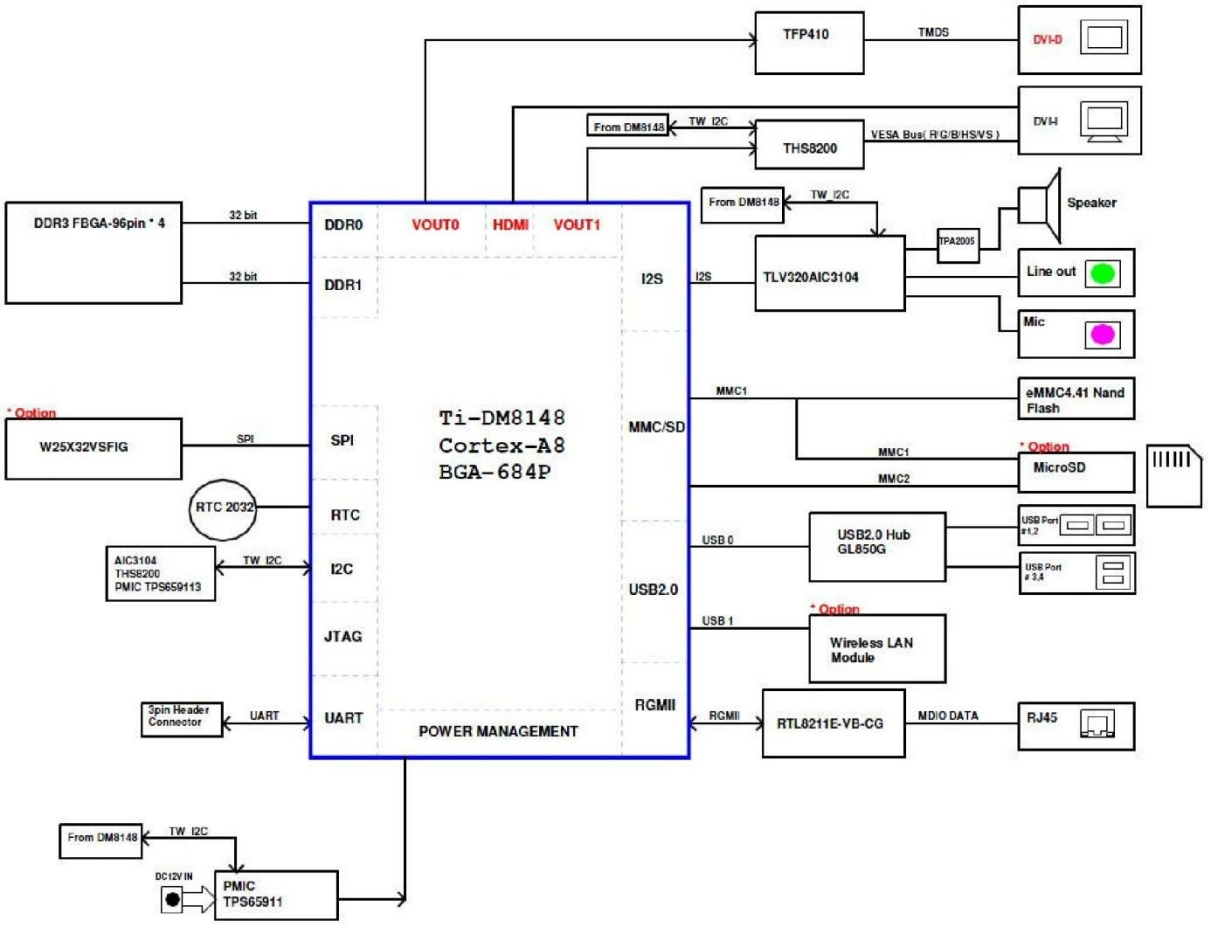


Rear Side View

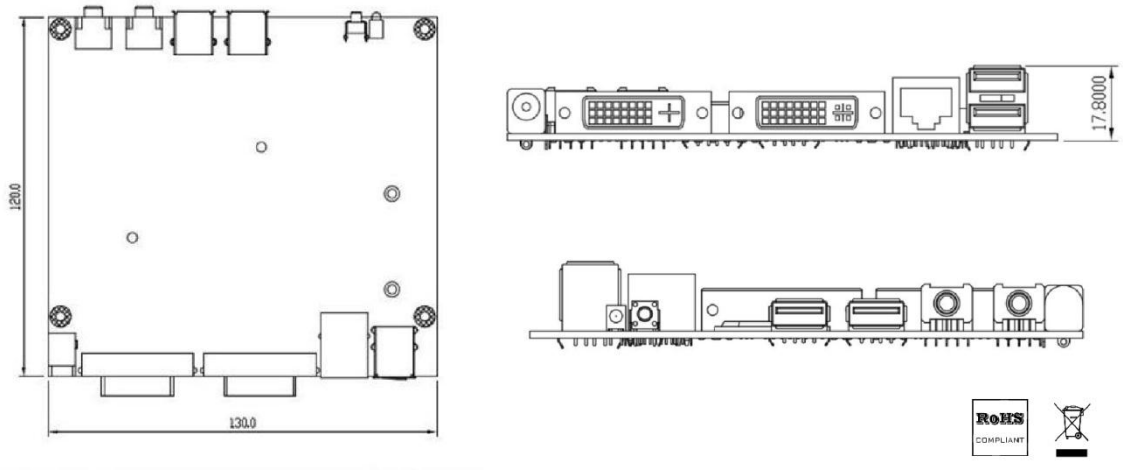




2.4 Block Diagram



2.5 Board Dimension Drawing



3. Power Consumption

3.1 Power Supply

Adapter Type, Spec. is 12V 2A 24W

3.2 Main Chip Power Consumption

Parameter	DC-IN (+12V)	+5VSUSU (+5V)	+3.3SUS (+3.3V)	VDDQ (+1.5V)	CVDD (+1.2V)	+5V	+3.3V	VTT	Amount Unit : W
DM8148									5W
RTL8211E							82.5mA		0.27W
DDR 3 (1024M) * 4				50mA Max:1W					4W
eMMC							150mA		
AIC3104									14mW
TFP410							120mA		0.396W
THS8200									
GL850G						85.3mA			0.4265W
USB2.0 Port * 4						2.0A			2W
Other						100mA			0.5W
Total									12.61W

4. Jumper and Connector

(9) PCB Assembly Top Side View

Figure 4-1 shows topside component placement drawing of LX TI DM8148 V: 1.0

Top:

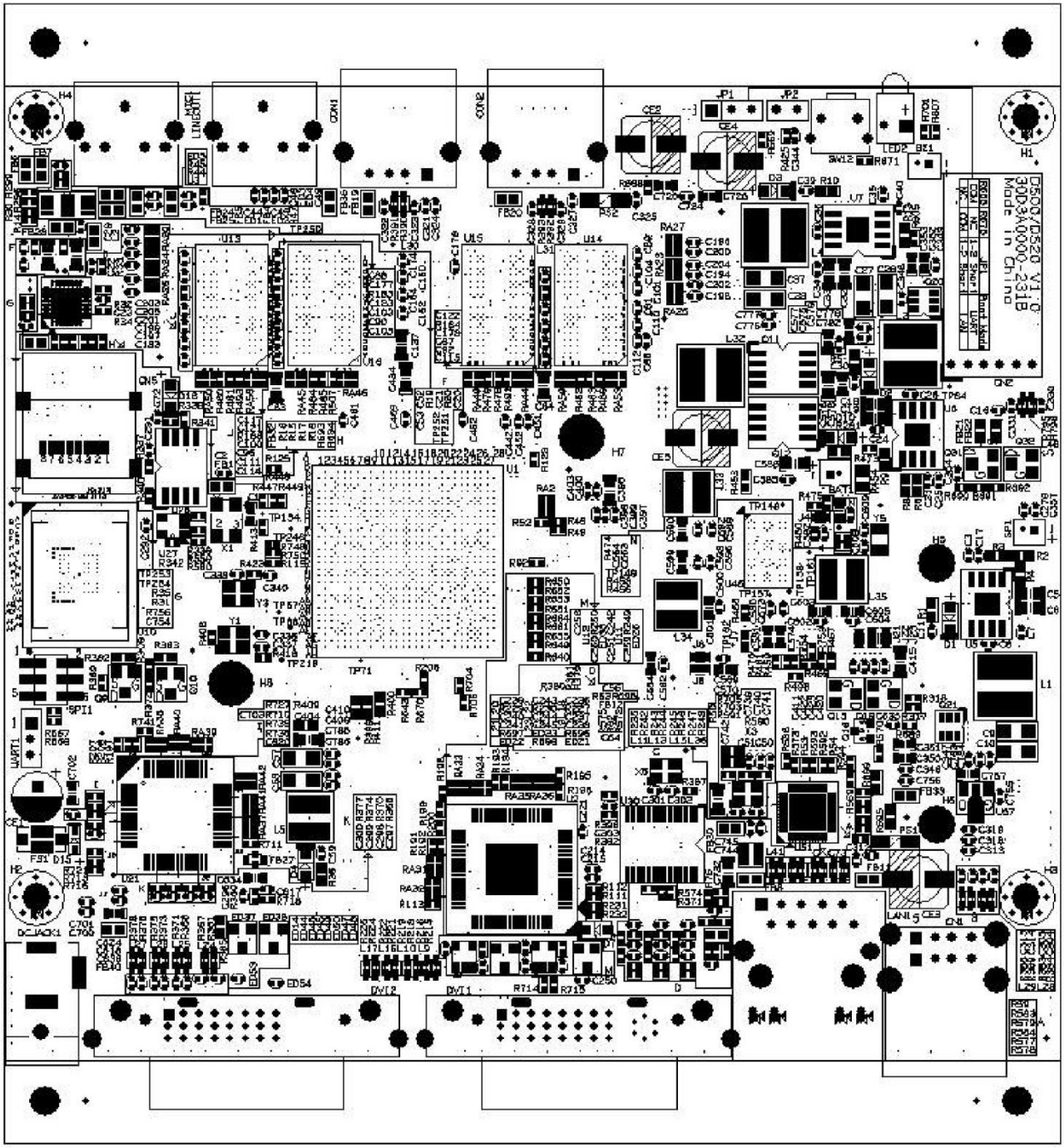


Figure 4-1

Bottom:

Figure 4-2 shows bottom side component placement drawing of LX TI DM8148 V: 1.0

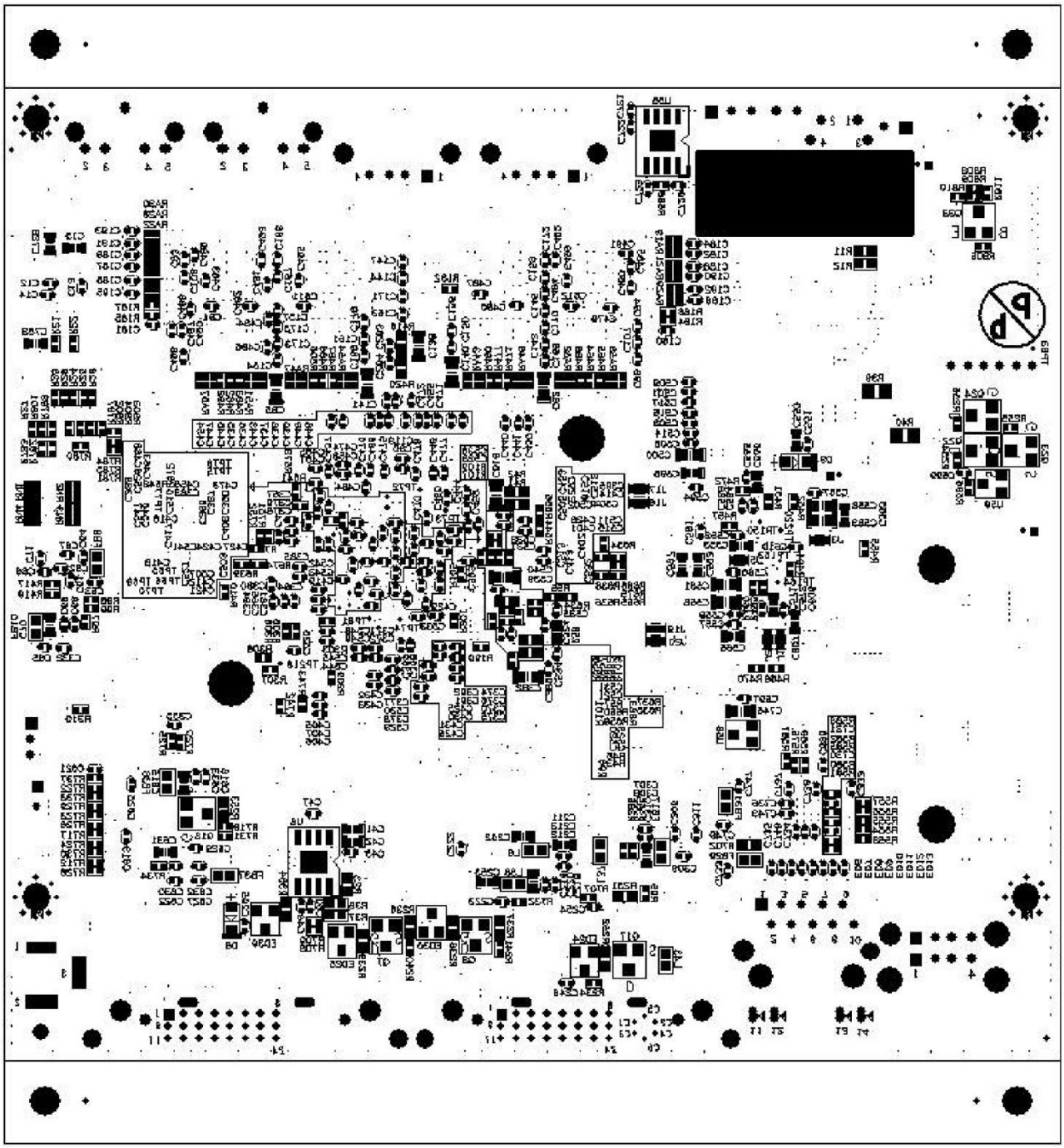


Figure 4-2

Front:

Figure 4-3 shows front side component placement drawing of LX TI DM8148 V:1.0

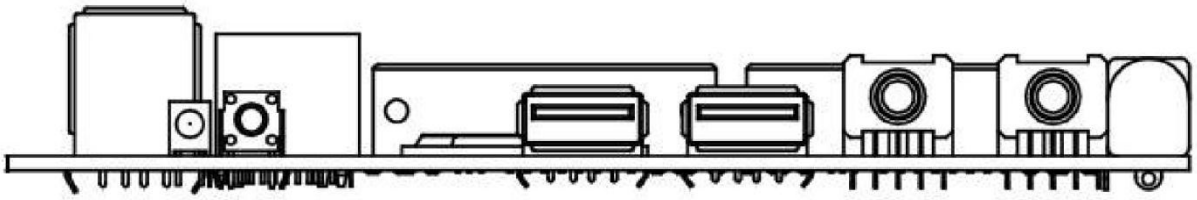


Figure 4-3

Rear:

Figure 4-4 shows rear side component placement drawing of LX TI DM8148 V:1.0

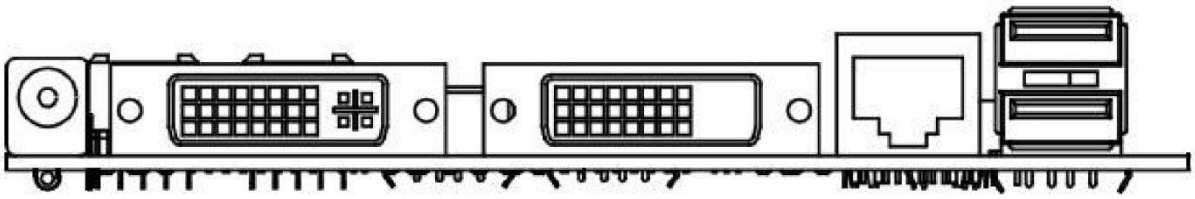
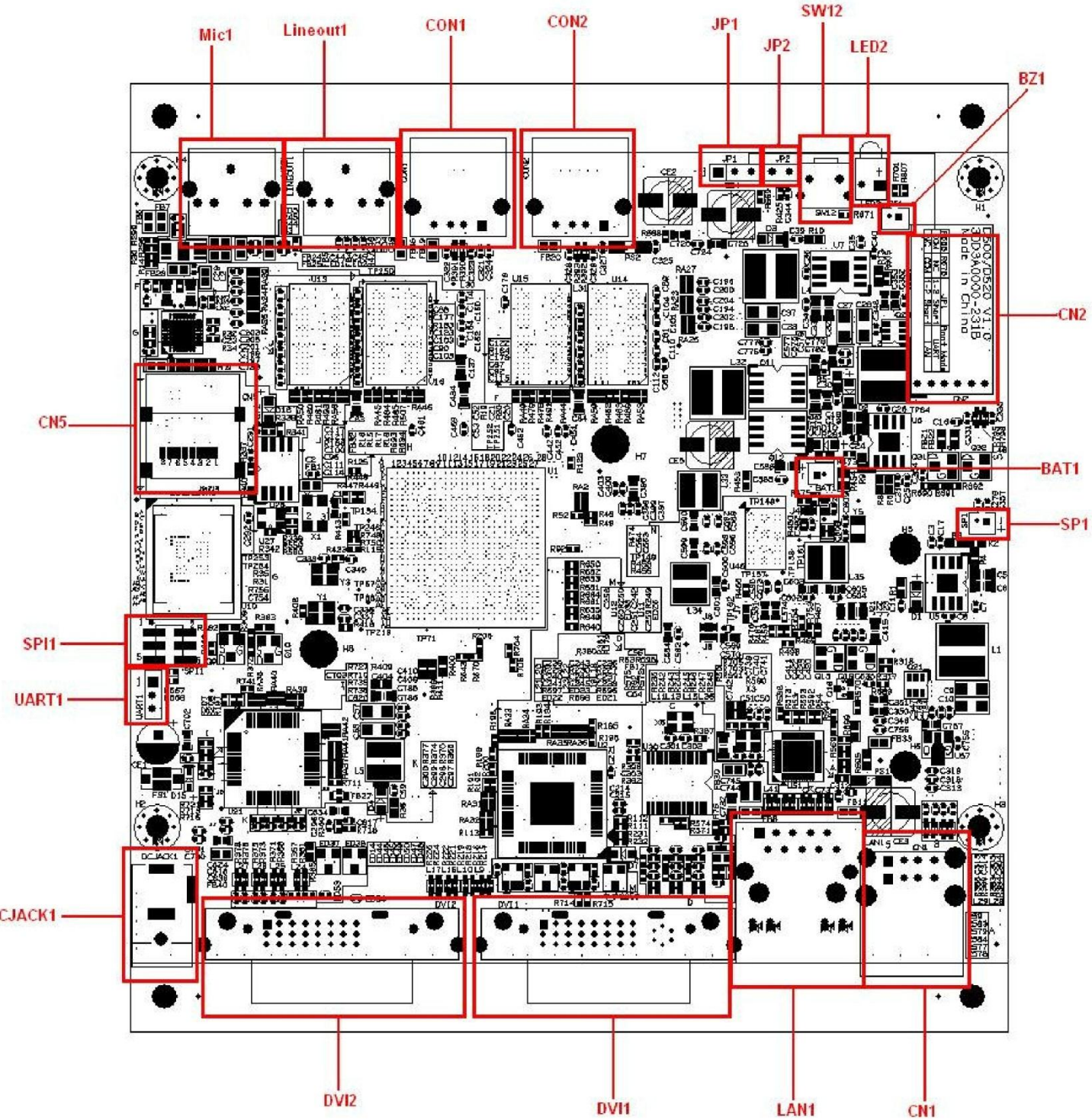


Figure 4-4

4.2 I/O Pin Define and Jumper Setting

4.2.1 PCBA internal IO Pin Definition



1. LINEOUT1 PIN Definition

No.	Definition	Description
1	AU_AGND	Headphone Jack Chassis Ground
2	AU_AGND	Headphone Jack Chassis Ground
3	LINEOUTL#	Headphone Audio Left Channel
4	LINEOUTR#	Headphone Audio Right Channel
5	HP_DET	Headphone detection

2. MIC1 Pin Definition

No.	Definition	Description
1	AU_AGND	Microphone Jack Chassis Ground
2	AU_AGND	Microphone Jack Chassis Ground
3	MIC_1N	Microphone Negative signal
4	MIC_1P	Microphone Positive signal
5	MIC_DET	Microphone detection

3. CON1 Pin Definition

No.	Definition	Description
1	USBPWR_2	CON1 VBUS +5V Power
2	Usb3_DT_n	USB Hub Port3 Negative signal
3	Usb3_DT_p	USB Hub Port3 Positive signal
4	GND_USB4	CON1 Chassis Ground

4. CON2 Pin Definition

No.	Definition	Description
1	USBPWR_2	CON2 VBUS +5V Power
2	Usb4_DT_n	USB Hub Port4 Negative signal
3	Usb4_DT_p	USB Hub Port4 Positive signal
4	GND_USB5	CON2 Chassis Ground

5. JP1 Pin Definition

No.	Definition	Description
1	N78554720	UART/ LAN Boot Mode Selection.
2	N81552656	System Ground
3	N.C	

6. JP2 Pin Definition

No.	Definition	Description
1	GND	System Ground
2	nRESPWRON2	Power off reset

7. SW12 Pin Definition

No.	Definition	Description
1	WAKE_UP#	External switch-on control(ON button) and define for Wake on LAN control too.
2	GND	System Ground
3	GND	System Ground
4	GND	System Ground

8. LED2 Pin Definition

No.	Definition	Description
C	LED2 Cathod	System Ground
A	LED2 Anode	+3.3V Pull high

9. BZ1 Pin Definition

No.	Definition	Description
1	Buzzer Positive	+5V Pull high
2	Buzzer Negative pin	Buzzer sound control

10. CN2 Pin Definition

No.	Definition	Description
1	LEDOUT	Reserve as test point
2	GND	System Ground
3	USB1_D_P1_T	DM8148 USB1 DP signal
4	USB1_D_N1_T	DM8148 USB1 DN signal
5	VOLATGE	3.3V system power
6	PDN	Reserve as test point

11. BAT1 Pin Definition

No.	Definition	Description
1	VBACKUP	RTC Battery input
2	GND	System Ground

12. SP1 Pin Definition

No.	Definition	Description
1	AMP_VOUT-	Speaker Negative pin
2	AMP_VOUT+	Speaker Positive pin

13. CN1 Pin Definition

No.	Definition	Description
1	USBPWR_1	CN1 VBUS +5V Power
2	Usb1_DT_n	USB Hub Port1 Negative signal
3	Usb1_DT_p	USB Hub Port1 Positive signal
4	GND	System Ground
5	USBPWR_1	CN1 VBUS +5V Power
6	Usb2_DT_n	USB Hub Port2 Negative signal
7	Usb2_DT_p	USB Hub Port2 Positive signal
8	GND	System Ground
9	GND	System Ground
10	GND	System Ground
11	GND	System Ground
12	GND	System Ground

14. LAN1 Pin Definition

No.	Definition	Description
1	+3.3VSUS(N.C)	3.3V Power pin
2	MDI0+	Positive of first Differential pair in 1000Base-T.
3	MDI0-	Negative of first Differential pair in 1000Base-T.
4	MDI1+	Positive of second Differential pair in 1000Base-T.
5	MDI1-	Negative of second Differential pair in 1000Base-T.
6	MDI2+	Positive of third Differential pair

		in 1000Base-T.
7	MDI2-	Negative of third Differential pair in 1000Base-T.
8	MDI3+	Positive of fourth Differential pair in 1000Base-T.
9	MDI3-	Negative of fourth Differential pair in 1000Base-T.
10	GND	System Ground

15. DVI1 Pin Definition

No.	Definition	Description
1	TX2-1A	HDMI Data 2 Differential Negative signal output
2	TX2+1A	HDMI Data 2 Differential Positive signal output
3	GND	System Ground
4	VGA_SCL	VGA EDID Serial Bus Clock
5	VGA_SDA	VGA EDID Serial Bus Data
6	DVI-I_SCL	DVI1 EDID Serial Bus Clock
7	DVI-I_SDA	DVI1 EDID Serial Bus Data
8	VS_VGA	VGA Vertical Synchronization
9	TX1-1A	HDMI Data 1 Differential Negative signal output
10	TX1+1A	HDMI Data 1 Differential Positive signal output
11	GND	System Ground
12	NC	No connection
13	NC	No connection
14	+5V_DVI-I	DVI1 5V Power
15	GND	System Ground
16	DVI-I_HPD	DVI-I Hot Plug Detection
17	TX0-1A	HDMI Data 0 Differential Negative signal output
18	TX0+1A	HDMI Data 0 Differential Positive signal output
19	GND	System Ground
20	NC	No connection
21	NC	No connection
22	GND	System Ground
23	TXC+1A	HDMI Clock Differential Negative signal output

24	TXC-1A	HDMI Clock Differential Positive signal output
C1	CRT_R	Analog output of Red DAC
C2	CRT_G	Analog output of Green DAC
C3	CRT_B	Analog output of Blue DAC
C4	HS_VGA	VGA Horizontal Synchronization
C5	CRT_AGND	CRT Analog Ground
C6	CRT_AGND	CRT Analog Ground

16. DVI2 Pin Definition

No.	Definition	Description
1	DVID_D2-	DVI Data 2 Differential Negative signal output
2	DVID_D2+	DVI Data 2 Differential Positive signal output
3	GND	System Ground
4	NC	No connection
5	NC	No connection
6	DVI-D_SCL	DVI2 EDID Serial Bus Clock
7	DVI-D_SDA	DVI2 EDID Serial Bus Data
8	NC	No connection
9	DVID_D1-	DVI Data 1 Differential Negative signal output
10	DVID_D1+	DVI Data 1 Differential Positive signal output
11	GND	System Ground
12	NC	No connection
13	NC	No connection
14	+5V_DVI-D	DVI2 5V Power
15	GND	System Ground
16	DVID_HPD	DVI-D Hot Plug Detection
17	DVID_D0-	DVI Data 0 Differential Negative signal output
18	DVID_D0+	DVI Data 0 Differential Positive signal output
19	GND	System Ground
20	NC	No connection
21	NC	No connection
22	GND	System Ground
23	DVID_CLK+	DVI Clock Differential Negative

		signal output
24	DVID_CLK-	DVI Clock Differential Positive signal output

17. DCJACK1 Pin Definition

No.	Definition	Description
1	DC12V	DC +12V Power input
2	GND	System Ground
3	GND	System Ground

18. UART1 Pin Definition

No.	Definition	Description
1	UART0_TXD	UART0 Transmit Data Output
2	UART0_RXD	UART0 Receive Data Input
3	GND	System Ground

19. SPI1 Pin Definition

No.	Definition	Description
1	SPI_3.3V	SPI ROM 3.3V Power
2	GND	System Ground
3	ROM_CSn	SPI ROM Chip Selection
4	SPI0_SCLK	SPI ROM Serial Clock Input
5	SPI0_MOSI	SPI ROM Serial Data Input
6	SPI0_MISO	SPI ROM Serial Data Output

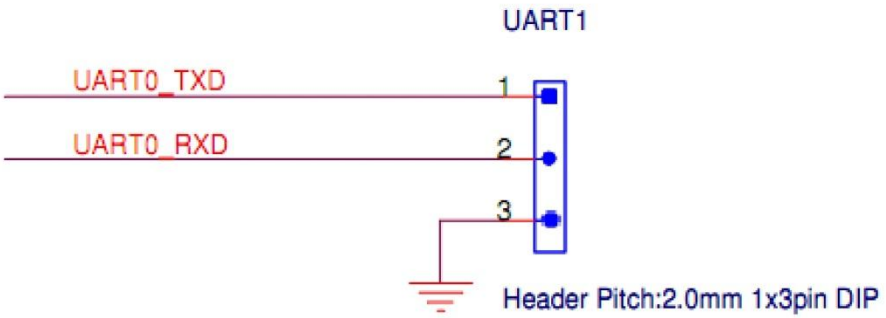
20. CN5 Pin Definition

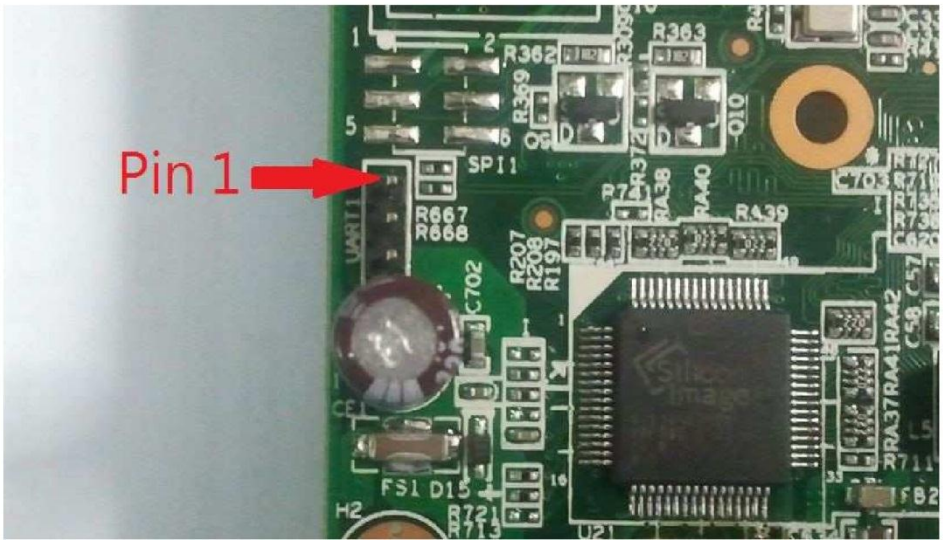
No.	Definition	Description
1	uSD_DAT2	MMC1 Data2 I/O.
2	uSD_DAT3	MMC1 Data3 I/O
3	uSD_CMD	MMC1 Command input
4	+3.3V	MMC1 3.3V Power
5	uSD_CLK	MMC1 Clock input
6	GND	System Ground
7	uSD_DAT0	MMC1 Data0 I/O.
8	uSD_DAT1	MMC1 Data1 I/O.

9	GND	System Ground
10	GND	System Ground
11	GND	System Ground
12	GND	System Ground

5. DEBUG PORT USAGE

There is a debug port noted as “UART1” on the boar d. To connect debug port with host, you can use *Chip PC USB-to-serial fixture* or make a similar cable by yourself. The pin definition of UART1 can be found as below:





If you use *Chip PC USB-to-serial fixture*, please download the VCP driver and install it on your host. The VCP driver can be found in the following link: http://www.ftdichip.com/Drivers/VCP.htm

You can use terminal emulator software such as Tera Term (http://logmett.com/index.php?/download/tera-term-474-freeware.html) to control the console interface on host side. Please remember set UART baud rate to **115200**, otherwise the terminal emulator can’t correctly show the console messages.